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Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L23

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Search History

DATE: Wednesday, September 21, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L23	L22 and l16	26	L23
L22	$synchroniz$[ab]	172045	L22
L21	L20 and l16	5	L21
L20	$synchroniz$[ti]	41741	L20
L19	L16 same stream	4	L19
L18	L6 same expect	8	L18
L17	L16 same bit	27	L17
L16	L15 same seed	70	L16
L15	$synchroniz$ same pattern	26531	L15
L14	pattern same bit same expect same stream	36	L14
L13	L2 same pattern	19	L13
L12	L2 same $synchroniz$	8	L12
L11	L8 same stream	21	L11
L10	l6 same l8	0	L10

L9	L8 same seed	7	L9
L8	expect adj1 data	556	L8
L7	L6 same l2	0	L7
L6	known adj1 pattern	3453	L6
L5	l2 same stream	3	L5
L4	L3 same (group or pattern)	17	L4
L3	L2 same value	32	L3
L2	seed same bit same expect$	50	L2
DB=USPT; PLUR=YES; OP=OR			
L1	6647523[pn] or 6477675[pn] or 6349399[pn]	3	L1

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L19: Entry 1 of 4 File: USPT Oct 21, 2003

DOCUMENT-IDENTIFIER: US 6636994 B1
TITLE: Apparatus and method for examining bit values during bit error location measurements

Detailed Description Text (3):
In the method of the invention, a user bit stream is selected for analysis. From this bit stream a seed bit segment is obtained, and a reference bit stream is generated from the seed bit segment by loading a linear feedback shift register (LFSR). Thereafter, the reference bit stream is synchronized with the user bit stream so that data in the user bit stream and the reference stream can be compared. Reference patterns and allowable data streams are not arbitrary sequences. Rather, they are in some way constrained allowing for an error detector to quickly synchronize and then to be able to create a local reference to use for bit comparisons during the actual error rate measurement.

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L9: Entry 6 of 7 File: USPT Aug 21, 2001

DOCUMENT-IDENTIFIER: US 6279090 B1
** See image for Certificate of Correction **
TITLE: Method and apparatus for resynchronizing a plurality of clock signals used in latching respective digital signals applied to a packetized memory device

Detailed Description Text (91):
The initialization sequencer 430 further includes a pattern generator 2108 receiving either the flag-latched word FLAT<0:3> or latched word D0L<0:3> from a multiplexer 2110, and utilizes the applied word to develop the synchronization sequence word SYNCSEQ<0:3>. As previously described, the SYNCSEQ<0:3> word is applied to the evaluation circuits 420 and 428 (FIG. 4) to determine the expect data for these circuits. The multiplexer 2110 applies the FLAT<0:3> word when the ICLK clock domain is being synchronized, and otherwise applies the D0L<0:3> word when either the IDCLK0 or IDCLK1 clock domains are being synchronized. A pattern generator clocking circuit 2112 clocks the pattern generator 2108 with a pair of complementary seed clock signals SCLK, SCLK, and also applies a seed signal SEED to the pattern generator 2108. In response to these signals, the pattern generator 2108 utilizes the FLAT<0:3> or D0L<0:3> word output by the multiplexer 2110 to develop the synchronization sequence word SYNCSEQ<0:3> which, as previously described, is applied to the evaluation circuits 420 and 428 (FIG. 4) to determine expect data for these circuits. The pattern generator clocking circuit 2112 is controlled by the initialization strobe generator 2100 and reset in response to the CNTRESET signal generated by the phase compare counter 2104.

Detailed Description Text (109):
The pattern generator clocking circuit 2112 couples the output of the NAND gate 2620 through inverters 2622 and 2624 to develop the pair of complementary seed clock signals SCLK, SCLK which, as previously described above, clock the pattern generator 2108 (FIG. 6) to generate sequential SYNCSEQ<0:3> words as it is clocked, each of the SYNCSEQ<0:3> words representing expect data corresponding to a particular captured command or data packet. A pulse generator 2626 applies a low output pulse through series connected inverters 2628 and 2630 to a first input of the NAND gate 2620. The pulse generator 2626 generates the low output pulse in response to a falling-edge transition from a NOR gate 2632. The NOR gate 2632 has one input coupled to ground and a second input coupled to the output of an RS flip-flop 2634 including cross-coupled NAND gates 2636 and 2638. The RS flip-flop 2634 receives the ACTIVE signal on a set input and the CNTREST signal on a reset input. In response to the CNTREST signal going low, the RS flip-flop 2634 is reset, driving the output of the NAND gate 2636 low which, in turn, causes the NOR gate 2632 to drive its output high. Once reset, the RS flip-flop 2634 is set in response to the ACTIVE signal going active low, causing the NAND gate 2636 to drive its output high which, in turn, causes the NOR gate 2632 to drive its output low.

Detailed Description Text (111):
In operation, the pattern generator clocking circuit 2112 operates in two modes, a seed mode and an expect data generation mode. For the following description, assume the CNTREST signal has just pulsed active low, resetting the RS flip-flop 2634 and RS flip-flop 2600. When the RS flip-flop 2600 is reset, the NAND gate 2604 drives its output low, causing the inverter 2608 to drive the SEED signal active high. When the RS flip-flop 2634 is reset, the NAND gate 2636 drives its output low,

causing the NOR gate 2632 to drive its output high. At this point, the pulse generator 2626 maintains its output high and this high output is applied through the inverters 2628 and 2630 to the NAND gate 2620. In addition, the positive-edge delay circuit 2642 applies a high output to the NAND gate 2640 in response to the high output from the inverter 2630. At this point, the NAND gate 2640 receives two high inputs so its output is low, but it is assumed the pulse generator 2644 has already generated its low output pulse in response to the falling-edge transition from the NAND gate 2640. Thus, the pulse generator 2644 maintains its output high and the NAND gate 2646, in turn, drives its output low, causing the inverter 2648 to apply a high output to the NAND gate 2620. The NAND gate 2620 likewise also receives two high inputs at this point and accordingly drives its output low, causing the inverters 2622 and 2624 to drive the SCLK signal high and SCLK signal low, respectively.

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L9: Entry 1 of 7 File: USPT Mar 2, 2004

DOCUMENT-IDENTIFIER: US 6700903 B1
TITLE: Upstream scrambler seeding system and method in a passive optical network

Detailed Description Text (9):
The present invention solves this problem. FIG. 5 is a flowchart of the method for utilizing new seed values for every upstream data transmission according to the preferred embodiment of the present invention. When transmitting upstream, i.e., from any of the ONUs 106 to the OLT 102 the ONU 106 generates 502 a data cell, e.g., an ATM cell. Then a seed is selected 504 that is known to both the OLT 102 and the ONU 106. The seed can be derived from a sequence previously agreed upon and known, or by some predictable fashion defined by the system. In one embodiment of the present invention, the seed is based upon the position of the cell within a transport frame. Since both the OLT 102 and the ONU 106 know the position of the cell within the transport frame a value relating to this position can be used as the seed. For example, an upstream frame may include 53 cells in an ITU G.983.1 compliant network. The seed for the each cell can be related to a value corresponding to the position of the cell in the frame. In will be apparent that many other seed generating techniques can be used. For example, the seed could be a simple count of the cell being sent by the ONU 106. Each transmission would increment this count, subject to higher-level synchronization. Alternatively, both the OLT 102 and ONU 106 could use an LFSR register to generate a random seed for each transmission, synchronized to the beginning of a frame boundary. An LFSR is a device which produces a pseudo-random sequence of numbers. Another alternative is that the seed could be taken from an element of the data last sent from ONU 106. For example, the seed for each station would be initialized to "one". When an ONU 106A sends a cell, the last 8-bits of data it sends are captured by the OLT 102, and saved to be used as the next descrambler seed when it expects data from ONU 106A.

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L9: Entry 5 of 7 File: USPT Jan 8, 2002

DOCUMENT-IDENTIFIER: US 6338127 B1
** See image for Certificate of Correction **
TITLE: Method and apparatus for resynchronizing a plurality of clock signals used to latch respective digital signals, and memory device using same

Detailed Description Text (55):
The initialization sequencer 430 further includes a pattern generator 2108 receiving either the flag-latched word FLAT<0:3> or latched word D0L<0:3> from a multiplexer 2110, and utilizes the applied word to develop the synchronization sequence word SYNCSEQ<0:3>. As previously described, the SYNCSEQ<0:3> word is applied to the evaluation circuits 420 and 428 (FIG. 4) to determine the expect data for these circuits. The multiplexer 2110 applies the FLAT<0:3> word when the ICLK clock domain is being synchronized, and otherwise applies the D0L<0:3> word when either the IDCLK0 or IDCLK1 clock domains are being synchronized. A pattern generator clocking circuit 2112 clocks the pattern generator 2108 with a pair of complementary seed clock signals SCLK, SCLK, and also applies a seed signal SEED to the pattern generator 2108. In response to these signals, the pattern generator 2108 utilizes the FLAT<0:3> or D0L<0:3> word output by the multiplexer 2110 to develop the synchronization sequence word SYNCSEQ<0:3> which, as previously described, is applied to the evaluation circuits 420 and 428 (FIG. 4) to determine expect data for these circuits. The pattern generator clocking circuit 2112 is controlled by the initialization strobe generator 2100 and reset in response to the CNTRESET signal generated by the phase compare counter 2104.

Detailed Description Text (73):
The pattern generator clocking circuit 2112 couples the output of the NAND gate 2620 through inverters 2622 and 2624 to develop the pair of complementary seed clock signals SCLK, SCLK which, as previously described above, clock the pattern generator 2108 (FIG. 6) to generate sequential SYNCSEQ<0:3> words as it is clocked, each of the SYNCSEQ<0:3> words representing expect data corresponding to a particular captured command or data packet. A pulse generator 2626 applies a low output pulse through series connected inverters 2628 and 2630 to a first input of the NAND gate 2620. The pulse generator 2626 generates the low output pulse in response to a falling-edge transition from a NOR gate 2632. The NOR gate 2632 has one input coupled to ground and a second input coupled to the output of an RS flip-flop 2634 including cross-coupled NAND gates 2636 and 2638. The RS flip-flop 2634 receives the ACTIVE signal on a set input and the CNTREST signal on a reset input. In response to the CNTREST signal going low, the RS flip-flop 2634 is reset, driving the output of the NAND gate 2636 low which, in turn, causes the NOR gate 2632 to drive its output high. Once reset, the RS flip-flop 2634 is set in response to the ACTIVE signal going active low, causing the NAND gate 2636 to drive its output high which, in turn, causes the NOR gate 2632 to drive its output low.

Detailed Description Text (75):
In operation, the pattern generator clocking circuit 2112 operates in two modes, a seed mode and an expect data generation mode. For the following description, assume the CNTREST signal has just pulsed active low, resetting the RS flip-flop 2634 and RS flip-flop 2600. When the RS flip-flop 2600 is reset, the NAND gate 2604 drives its output low, causing the inverter 2608 to drive the SEED signal active high. When the RS flip-flop 2634 is reset, the NAND gate 2636 drives its output low,

causing the NOR gate 2632 to drive its output high. At this point, the pulse generator 2626 maintains its output high and this high output is applied through the inverters 2628 and 2630 to the NAND gate 2620. In addition, the positive-edge delay circuit 2642 applies a high output to the NAND gate 2640 in response to the high output from the inverter 2630. At this point, the NAND gate 2640 receives two high inputs so its output is low, but it is assumed the pulse generator 2644 has already generated its low output pulse in response to the falling-edge transition from the NAND gate 2640. Thus, the pulse generator 2644 maintains its output high and the NAND gate 2646, in turn, drives its output low, causing the inverter 2648 to apply a high output to the NAND gate 2620. The NAND gate 2620 likewise also receives two high inputs at this point and accordingly drives its output low, causing the inverters 2622 and 2624 to drive the SCLK signal high and SCLK signal low, respectively.

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